

INFORMATION
DISCLOSURE
STATEMENT BY APPLICANT

Sheet 1 of 2



Application Number: 10/768,754
Filing Date: January 26, 2004
First Named Inventor: Adrian STOICA, et al.
Group Art Unit: Unknown
Examiner Name: Unknown
Attorney Docket Number: NPO-20535-2-CU

Examiner
Initials

NON PATENT LITERATURE DOCUMENTS


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Examiner's Signature:

Date Considered:

6/5/06

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Sheet 2 of 2		Application Number: 10/768,754 Filing Date: January 26, 2004 First Named Inventor: Adrian STOICA, et al. Group Art Unit: Unknown Examiner Name: Unknown Attorney Docket Number: NPO-20535-2-CU	
Examiner Initials	NON PATENT LITERATURE DOCUMENTS		
3	ZEBULUM, RICHARD S., et al., "Evolvable Systems in Hardware Design: Taxonomy, Survey and Applications," <i>Proc. Of the First Int'l. Conf. On Evolvable Systems</i> , Springer-Verlag, Japan, 1996, pp. 344-358.		
3	ZEBULUM, RICHARD S., et al., "Analog Circuits Evolution in Extrinsic and Intrinsic Modes," <i>Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware</i> , Springer-Verlag, Berlin, 1998, pp. 154-165.		
Examiner's Signature: 		Date Considered: 6/5/04	
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FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

Attorney Docket No.: NPO-20535-2-CU Serial No.: To be Assigned

Applicant(s): Adrian STOICA, et al.

Filing Date: Herewith

Group: Unknown

LIST OF PRIOR ART CITED BY APPLICANT

(Use several sheets if necessary)

U. S. PATENTS

Initials	Patent No	Issue Date	Name	Class	Subclass	Filing Date
3	US-5,258,947	11-02-1993	SOURGEN	365	96	12-07-1990
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3	US-6,363,517	03-26-2002	LEVI ET AL.	716	16	06-17-1999
3	US-6,363,519	03-26-2002	LEVI ET AL.	716	16	06-17-1999
3	US-6,378,122	04-23-2002	LEVI ET AL.	716	16	06-17-1999

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Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)				
3	Augusto, Soares J.A., and Almeida, Beltran C.F., "Analog Fault Diagnosis in Nonlinear DC Circuits with an Evolutionary Algorithm," <i>IEEE</i> , July 2000, pp. 609-616.				
3	Layzell, Paul, "A New Research Tool for Intrinsic Hardware Evolution," Second International Conference, <i>ICES98</i> , Lausanne, Switzerland, Springer, September 23-25, 1998, pp. 47-56.				

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Perkowski, M. Chebotarev, A., and Mishchenko, A., "Evolvable Hardware or Learning Hardware? Induction of State Machines from Temporal Logic Constraints," *Proceedings of the First NASA/DoD Workshop*, July 19-21, 1999, pp. 129-138.

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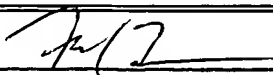
Initials	Patent No	Issue Date	Name	Class	Subclass	Filing Date

FOREIGN PATENT DOCUMENTS

Initials	Document Number	Date	Country	Name	Translation? (Yes/No/n/a)

Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)
2	Stoica, A., Keymeulen, D., Zebulum, R., Thakoor, A., Daud, T., Klimeck, G., Jin, Y., Tawel, R., and Duong, V., "Evolution of analog circuits on Field Programmable Transistor Arrays," <i>IEEE</i> , July, 2000, pp. 1-10.
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